REMARKS

STATUS OF CLAIMS

Claims 1-31 are pending.

Claim 11 is added and new claims 32-36 are added.

Thus, claims 1-36 remain pending for reconsideration, which is respectfully requested.

No new matter has been added in this Amendment. The foregoing rejections are hereby traversed.

REJECTIONS UNDER 35 U.S.C. §112:

Claim 11 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Accordingly claim 11 has been amended taking into consideration the Examiner's comments. Withdrawal of the indefiniteness rejection is respectfully requested.

REJECTIONS UNDER 35 U.S.C. §102(e)

Claims 1-31 are rejected under 35 U.S.C. §102(e) as being anticipated by Ikegawa (US Patent No. 6,538,758). Generally, new claims 32-36 are added to provide alternative recitations of independent claims 1 and 24. In particular, support for claim 35 can be found, for example, in page 30, line 25 to page 32, line 14, of the present Application.

Ikegawa (US Patent No. 6,538,758) discloses requesting re-transmitting image data when a bus reset occurs during a data transfer to maintain a printer output properly.

In contrast to Ikegawa, the present invention (claims 1-12 and new claim 32) is directed to an interface that determines whether a bus reset sequence, which is initiated based on a bus reset, has been performed normally, and transfers data to a host controller when the bus reset sequence has been performed normally. More particularly, for example claim 1, clearly recites "analyzing data provided from the external bus during the bus reset sequence and for determining whether the bus reset sequence has been completed normally, wherein the analysis circuit provides the data to the host controller when the bus reset sequence has been completed normally." Therefore, the claimed invention clearly provides "determining whether the bust reset sequence has been completed normally." Ikegawa does not disclose or suggest such bus reset error determination. In other words, Ikegawa only detects occurrence of a bus reset, but does not provide the present invention's "determining whether the bus reset

sequence has been completed normally." See, Ikegawa, FIG. 4, step 8, and column 15, line 55 to column 16, line 38.

Furthermore, the present invention (as recited in claims 13-31, and new claims 33 and 34) performs self-diagnosis prior to a predetermined connection procedure, and does not perform the predetermined connection procedure when an abnormality of a network is detected. That is, the present invention determines whether a bus reset sequence has been performed normally, or a circuit itself is normal, prior to a predetermined connection procedure (e.g. a bus reset). Again, Ikegewa, does not disclose or suggest, for example, the claim 13 recitation, "a self-diagnosis circuit for performing self-diagnosis of the interface prior to the predetermined connection procedure, wherein the interface suspends transition to the predetermined connection procedure when the self-diagnosis circuit generates a diagnosis indicating an abnormality of the interface." See also, claim 24, and new claim 33.

Therefore, the present invention is quite different from Ikegewa that detect a bus reset and re-generates a data transfer request on the assumption that the bus reset was normal.

In view of the claim amendment and the remarks, it is believed that the application is in condition for allowance, which is respectfully requested.

CONCLUSION

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

Respectfully submitted,
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